

04/30/2002

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LSI LOGIC-IP DEPT./4084337460 → 9170374672

NO. 483

0004



PTO/SB/05A (10-98)

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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				<i>Complete if Known</i>	
				Application Number	10/015,194
				Filing Date	November-20, 2001
				First Named Inventor	Jam s S. Koford
				Group Art Unit	2184-2125
				Examiner Name	
Sheet	1	of	1	Attorney Docket No.	/ 01-390

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where	T
aa		Simplify Programmable-Logic-IP Integration - Author(s) - Cravotta, Robert	
aa		Altera Casts Spotlight On IP Integration Tool - Author(s) - Souza, Crista	

Examiner signature		ALBERT W. PALADINO PATENT EXAMINER	Date considered	6-7-05
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05/13/2003

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NO. 659 0004



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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Group Art Unit	2184 2125
Examiner Name	
Attorney Docket No.	/ 01-390

Sheet 1 of 1

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code (if known)			
AW		5,222,030		Dangelo et al.	06-22-1993	
AW		6,574,778		Chang et al.	06-03-2003	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where	T
AW		"Rapid Chip Management System"; Filed November 20, 2002; US Serial #10/301,182 - Author(s) - DANIEL M. WEED	

Examiner signature	<i>Albert W. Paladino</i>	ALBERT W. PALADINO PATENT EXAMINER	Date considered	6-7-03
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06/30/2003

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LSI LOGIC-IP DEPT./4084337460 → 917037461

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PTO/S2/08A (10-98)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	10/015,194
Filing Date	November-20, 2001
First Named Inventor	James S. Koford
Group Art Unit	2184 2125
Examiner Name	
Attorney Docket No.	/01-390

Sheet 1 of 1

U.S. PATENT DOCUMENTS

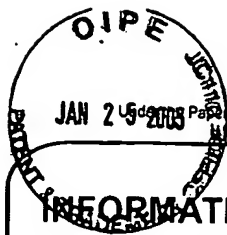
Examiner Initials	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code (if known)			
AMM		5,553,002		Dangelo et al.	09-03-1996	

Examiner signature	<i>Albert W. Paladino</i>	ALBERT W. PALADINO PATENT EXAMINER	Date entered	6-7-05
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Application Number	10/015,194
Filing Date	November-20, 2001
First Named Inventor	James S. Koford
Group Art Unit	2484 2125
Examiner Name	
Attorney Docket No.	/ 01-390

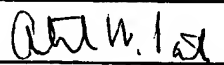
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U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code (if known)			
anp		5,553,002		Dangelo et al.	09-03-1996	
anp		6,678,875		Pajak et al.	01-13-2004	
anp		6,721,922		Walters et al.	04-13-2004	
anp		6,742,165		Lev et al.	05-25-2004	
anp		2003009724		Koford et al.	05-22-2003	
anp		2004002511		Chris Hamlin	02-05-2004	
anp		6,634,008		Dole	10-14-2003	
anp		6,704,917		Curran et al.	03-09-2004	
anp		6,269,467		Cheung, Cyrus C. (Hercules,	06-10-2003	
anp		6,253,358		Shuji Takahashi	06-26-2001	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where	T
anp		"A rule based VLSI process flow validation system with macroscopic process simulation", IEEE Transactions on semiconductor manufacturing, vol. 3, no. 4, November 1990, oages 239-246 - Author(s) - Funakoshi et al.	

Examiner signature		ALBERT W. PALACHEN PATENT EXAMINER	Date considered	6-7-05
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